What is claimed is:

1. A method for removal of hemispherical grained silicon in a deep trench, comprising the steps of:

forming an etch stop layer in a collar region of a trench on a substrate;

forming a hemispherical grained silicon (HSG) layer on the trench and the etch stop layer;

forming an arsenic silicon glass (ASG) layer on the HSG layer;

forming a photoresist layer at the bottom of the trench;

removing an upper ASG layer uncovered by the photoresist layer; and

removing an upper HSG layer uncovered by the photoresist layer.

2. The method of claim 1, further comprising the steps of:

removing the photoresist layer;

forming a cap layer on the trench;

forming a buried plate in the trench;

removing the residual ASG layer and the cap layer; and

forming a dielectric layer.

3. The method of claim 1, wherein the etch stop layer is a buried silicon germanium (SiGe) layer.

4. The method of claim 3, wherein the buried SiGe layer is further served as a mask for forming a bottle-shape trench.

5. The method of claim 3, wherein the buried SiGe layer is formed in the upper part of the trench by implanting germanium atoms into the silicon trench with a predetermined angle.

6. The method of claim 5, wherein the predetermined angle is from about 8 degrees to about 12 degrees.

7. The method of claim 3, wherein the buried SiGe layer is further formed in the upper part of the trench by rapid thermal annealing.

8. The method of claim 1, wherein the step of removing an upper HSG layer uncovered by the photoresist layer comprises a wet etch process.

9. The method of claim 8, wherein the wet etch process comprises employing a potassium hydroxide (KOH)/propanone/water etchant.

10. The method of claim 9, wherein a component ratio of the potassium hydroxide/propanone/water etchant is between around 0.8/1/3.5 and around 1.2/1/4.2, while the component ratio is equal to around 1/1/4, and an etch rate selectivity for the HSG layer and the buried SiGe layer is up to 20:1 by the etchant.

11. The method of claim 1, wherein the step of forming the HSG layer and the ASG layer comprises using a deposition process.

12. The method of claim 1, wherein the step of removing an upper ASG layer

uncovered by the photoresist layer comprises a wet etch process.

13. A method for manufacturing a trench capacitor, comprising the steps of:

providing a substrate having at least one trench structure;

forming an etch stop layer in an upper part of the trench on the substrate;

depositing a hemispherical grained silicon (HSG) layer on the trench and the etch stop layer;

depositing an arsenic silicon glass (ASG) layer on the HSG layer;

coating and recessing a photoresist layer on a bottom of the trench;

removing an upper ASG layer uncovered by the photoresist layer;

removing an upper HSG layer uncovered by the photoresist layer;

removing the photoresist layer;

depositing a cap layer on the trench;

forming a buried plate in the trench;

recessing the residual ASG layer and the cap layer; and

depositing a dielectric layer.

14. The method of claim 13, wherein the etch stop layer is a buried silicon germanium (SiGe) layer.

15. The method of claim 14, wherein the buried SiGe layer is further served as a mask for forming a bottle-shape trench.

16. The method of claim 14, wherein the step of forming the buried SiGe layer further comprises:

implanting germanium atoms into the upper part of the trench with a predetermined angle; and

employing rapid thermal annealing.

17. The method of claim 13, wherein the step of removing an upper HSG layer uncovered by the photoresist layer comprises a wet etch process.

18. The method of claim 17, wherein the wet etch process comprises employing a potassium hydroxide (KOH)/propanone/water etchant.

19. The method of claim 13, wherein the step of forming a buried plate comprises annealing the ASG layer to drive arsenic atoms into the trench.

20. The method of claim 13, wherein the cap layer comprises a tetra ethyl ortho silicate (TEOS) layer.

21. The method of claim 13, wherein the dielectric layer comprises an oxide layer and a nitride layer.